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Design of 5.5 GHz Highly Linear CMOS Low Noise Amplifier

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Taschenbuch. Book Condition: Neu. 220x150x5 mm. This item is printed on demand - Print on Demand Neuware - Recently, telecommunication system requires high performance, low noise, low power and high linear RF circuits. Since the digital modulation design requires highly linear front end circuits, the linearity requirement of the LNA becomes more rigorous. Due to possible large interference signal tones at the receiver end along with the carrier, LNA is expected to provide high linearity, thus preventing the intermodulation tones created by the interference signal from corrupting the carrier signal. The research focuses on designing a LNA which achieves high linearity without sacrificing any of its specifications of gain and Noise Figure (NF). The project focused on designing a 5.5 GHz linear LNA using a standard UMC.18um technology. The LNA employed inductive source degeneration topology with on chip passive spiral inductor. Employing the body biasing technique with post distortion scheme not only achieve high linearity, but also minimizes the degradation of gain, noise figure and power consumption. The simulation results show that CMOS tech has the capability to achieve a 5.5 GHz LNA. The LNA draws a 10.8mw power on 1.8V power supply...



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